Journal of Nano- and Electronic Physics
Vol. **13** No 4, 04021(5pp) (2021)

Журнал нано- та електронної фізики
Том **13** № 4, 04021(5cc) (2021)

Study of a New Device Structure: Graphene Field Effect Transistor (GFET)

P. Vimala[1,*], Manjunath Bassapuri[1], C.R. Harshavardhan[1], P. Harshith[1], Rahul Jarali[1], T.S. Arun Samuel[2]

[1] *Department of Electronics & Communication Engineering, Dayananda Sagar College of Engineering, Shavige Malleshwara Hills, Bengaluru, 560078 Karnataka, India*
[2] *National Engineering College, Kovilpatti, 628503 Tamil Nadu, India*

(Received 29 March 2021; revised manuscript received 09 August 2021; published online 20 August 2021)

The aim of this paper is to improve the performance of nanodevices yielding the overall gain of electronic applications. The performance in low-power consumption, high sensitivity and faster switching speeds are prerequisites for the modern era of electronics. The proposed paper defines the 3D structure of a Graphene Field Effect Transistor (GFET). The titled structure is in an evolutionary phase and is being researched day by day. The prime advantages of the device for its overall performance and specific applications have made a detailed study interesting. The structure of graphene provides exceptional capabilities for its operation and hence an excellent solution for sensing applications. Graphene is placed between the source and drain junctions, forming a bridge and providing a path for electron movement. The nanodevice is simulated for electrical parameters such as drain current, drain voltage, Dirac voltage, mobility, electron density, hole density, temperature. The device is modelled using the NanoHUB simulation tool. The behavior of drain current with varying channel length and gate voltages is proposed. The improved characteristics of the device with decreasing channel length, gate voltage and Dirac point shift are observed. The Dirac point plays a vital role in the conduction mechanism of graphene and hence GFET. The Dirac point was studied for the given simulation parameters, and the Dirac point shift was observed, leading to a change in conduction. The variation of drain current was simulated for different drain voltages, which provides us sufficient evidence of efficiency and hence low-power consumption. The distribution of carriers and various operating temperatures along the channel is presented for a varying gate voltage. The results show the outperformance of GFET for present day needs in sensing applications.

Keywords: NanoHUB, Graphene, GFET, Mobility, Drain current.

DOI: 10.21272/jnep.13(4).04021 PACS numbers: 72.80.Vp, 85.30.Tv

1. INTRODUCTION

A tremendous increment in the efficiency demand in the electronics industry has led to the transition to more advanced devices. A conventional semiconductor device, a transistor manufactured in the last century, now faces limitations to keep up with the current trend [1]. A new nanodevice, a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) operating in a different mode (electric field, as the name indicates), was proposed and fabricated. The need to reduce the bulge size of PCs, laptops and other electronic devices which is ultimately the result of reducing the transistor size, was a big deal. The eminent scientist Gordon Moore stated that the number of transistors in an integrated chip doubles every 18 months. The scaling of MOSFETs was done based on Moore's law and thus reduced the channel length. Reducing the channel length eventually gave rise to numerous limitations called short-channel effects and decaying parasitic effects [2]. In the recent times, we have faced a problem called latch-up; this is a drawback of the CMOS technology used for manufacturing conventional MOSFETs [3]. A new fabrication process named SOI technology which reduces latch-up by creating a physical barrier between *p*-*n*-*p*-*n* junction, reducing parasitic effects. It is also concluded that Moore's law is inappropriate since it was practically found that we cannot further reduce the channel length [4]. Efforts are being made to reduce the short-channel effects which have led to the discovery of other nanodevices such as MUGFET [5-7], FinFET [8], tunnel FET [9], nanowire TFET [10], and so on. The need for high accuracy in bonding and reactions at the atomic level fits graphene for this role [11, 12]. The distribution of electrons in graphene makes it the best carbon allotrope. Graphene, having a single layer of carbon atoms at its surface, overcomes the limitations in biomedicine and sensing industry [13-15].

In our study, we consider the operation of a GFET in terms of electrical parameters. The GFET structure is simulated to get possible outcomes, the plots of the drain current are plotted for different channel lengths and gate voltages. Others include plots of electron density, hole density, temperature with respect to position. Section II deals with the proposed device structure and its characteristics. Section III consists of the obtained results and discussion, showing electrical parameters and their effect on the GFET performance.

2. PROPOSED STRUCTURE

Fig. 1 illustrates the proposed structure of a GFET, which is one of the devices contributing to SOI technology. GFETs are devices with high sensible applications. The source and drain are *p*-doped, and the substrate is *n*-doped. The substrate made of silicon is compressed by silicon dioxide as a buried insulator above it. Graphene forms a channel region between the source and drain junctions. Graphene is a monolayer used for conduction, above which is the gate oxide and then the gate termi-

* drvimala-ece@dayanandasagar.edu

nal, which is a key to operate the device. GFET parameters include channel length (L), channel width (W), gate oxide (t_{ox}), and buried oxide (t_{box}). GFET device is modeled and simulated by NanoHUB software and the output values are plotted in MATLAB. The predefined values used in the simulation are tabulated in Table 1.

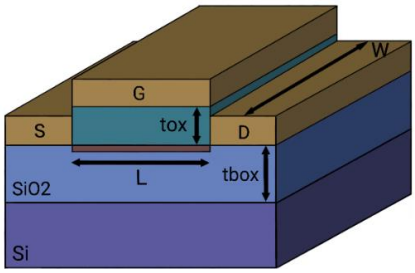

Fig. 1 – The 3D structure of a GFET

Table 1 – Tabulation of parameters for a GFET

S. No	Parameter	Symbol	Value
1.	Channel width	W	10^{-6} m
2.	Channel length	L	10^{-6} m
3.	Initial temperature	T	293 K
4.	Top gate oxide thickness	t_{ox}	10^{-8} m
5.	Mobility	μ	3000 cm²/Vs
6.	Back gate oxide thickness	t_{box}	$3{\cdot}10^{-7}$ m
7.	Metal contact resistance	Ω	350 Ohm·μm²
8.	Thermal conductivity of insulator	σ_{ox}	1.3 W/m/K
9.	Thermal conductivity of wafer substrate	σ_{si}	100 W/m/K
10.	Thermal conductivity of graphene	σ_G	1000 W/m/K

3. RESULTS AND DISCUSSION

Fig. 2 shows the change in the drain current (I_d) with the drain voltage (V_d) for different channel length. The current in milliampere (mA) along the vertical axis varies with the voltage in volt (V) along the horizontal axis. Solid lines indicate the channel length of 1 μm, whereas dashed lines indicate a 0.5 μm channel length. The current (I_d) increases linearly with voltage (V_d), the current (I_d) for a 0.5 μm channel length reaches a peak value of about 1 mA for a driving force of 2 V, whereas the current (I_d) for a 1 μm channel length reaches a peak value of 1 mA for a driving force equal to 3 V.

Fig. 3 depicts the variation of drain current (I_d) with drain voltage (V_d) for different gate voltage (V_g). The current in milliampere (mA) plotted along the vertical axis varies with the voltage in volt (V) along the horizontal axis. Solid lines indicate that V_g is maintained at 0 V, dotted lines indicate V_g is maintained at 0.5 V, and dashed lines indicate V_g is at 1.5 V. The current varies linearly with voltage for the applied V_g. The current (I_d) for a 0 V gate voltage reaches a peak value of 1 mA for a driving force of nearly 3 V, similarly the device reaches 1 mA for V_d of 2.5 and 2 V, respectively, for dotted and solid lines.

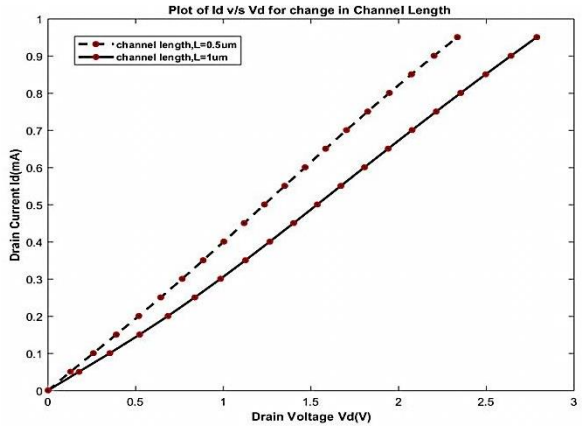

Fig. 2 – Variation of drain current with channel length

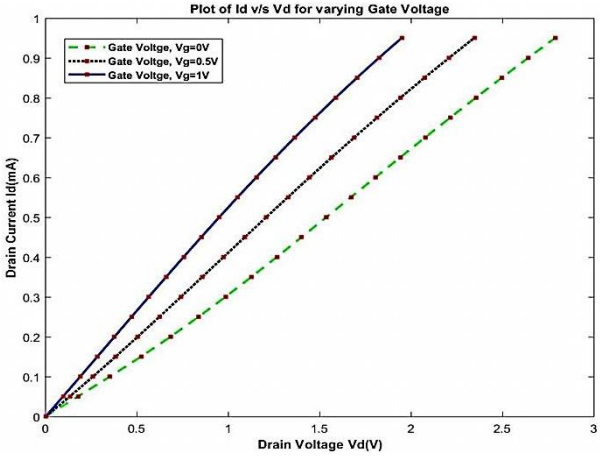

Fig. 3 – Variation of drain current for three different gate voltages

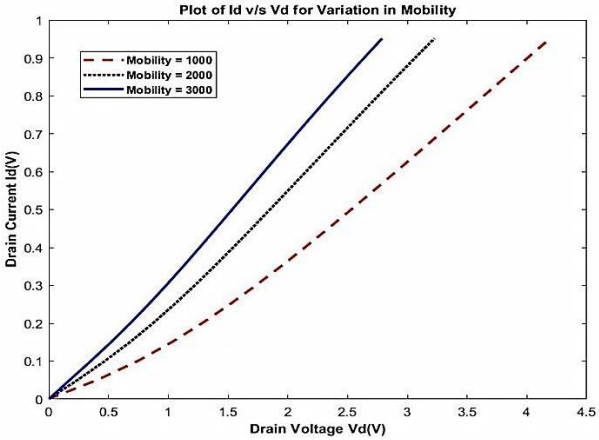

Fig. 4 – Variation of drain current for different electron mobilities

Fig. 4 shows the variation of drain current (I_d) with drain voltage (V_d) for various mobility values. The drain current (mA) is plotted along the vertical axis and the drain voltage (V) – along the horizontal axis. The solid line represents an electron mobility of 3000 cm²/V·s, the curve depicts a linear increase in current with respect to voltage, and a peak current of approximately 1 mA is achieved for a driving voltage of approximately 2.5 V. The dotted line represents an electron mobility of 2000 cm²/V·s, and the curve depicts a linear increase in drain current with respect to drain voltage. The peak

current value of 1 mA is achieved for a driving force of approximately 3.5 V. The dashed line represents an electron mobility of 1000 $cm^2/V{\cdot}s$, and a similar characteristic curve was observed, resulting in a peak current value of 1 mA for a driving force of approximately 4.5 V.

Fig. 5 shows the variation of electron density versus position. The density of electrons (in cm^{-2}) is plotted along the vertical axis and the position (in μm) – along the horizontal axis. The dashed line, dotted line and solid line in the graph indicate that the gate voltage (V_g) is maintained at 0, 1 and 2 V, respectively. When zero V_g is applied, there is a drift of electrons which form a channel between source and drain. The density varies from $0.5{\cdot}10^{16}$ cm^{-2} in the source to $5.5{\cdot}10^{16}$ cm^{-2} in the channel. When a small V_g, say 1 V, is applied, more electrons tend to be excited, and the density varies from $2.2{\cdot}10^{16}$ cm^{-2} in the source to $6{\cdot}10^{16}$ cm^{-2} in the channel. Similarly, when 2 V is applied through the gate, the density increases from $4.5{\cdot}10^{16}$ cm^{-2} to $7{\cdot}10^{16}$ cm^{-2}. In all three cases, there is a tremendous increase in the number of electrons per cm^2.

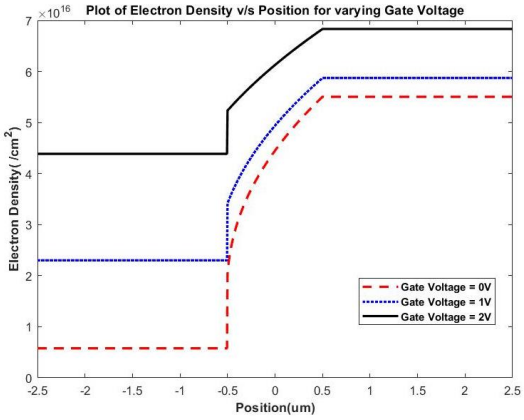

Fig. 5 – Variation of electron density in the channel region for different gate voltage

Fig. 6 shows the variation of hole density versus position. The density of holes (in cm^{-2}) is plotted along the vertical axis and the position (in μm) – along the horizontal axis. The dotted line, dashed line and solid line in the graph indicate that the gate voltage (V_g) is maintained at 0, 1 and 2 V, respectively. Before the application of V_g, the holes had a maximum concentration, resulting in the initial density of $6{\cdot}10^{16}$ cm^{-2} on the source side, and decreased suddenly in the channel region, resulting in $1{\cdot}10^{16}$ cm^{-2}. When a voltage of 1 V is applied to the gate region, the hole density decreases from $1.5{\cdot}10^{16}$ cm^{-2} in the source to $1{\cdot}10^{16}$ cm^{-2} in the channel. Similar characteristics are observed when V_g is held at 2 V, the hole density decreases from $0.9{\cdot}10^{16}$ to $0.5{\cdot}10^{16}$ cm^{-2}, and the number of electrons, on the contrary, increases.

Fig. 7 depicts different temperature ranges with respect to position. The temperature (in K) is plotted along the vertical axis and the position (in μm) – along the horizontal axis. The dotted line, dashed line and solid line in the graph indicate that the gate voltage (V_g) is maintained at 0, 1 and 2 V, respectively. In the device, before V_g ($V_g = 0$ V) is applied, there will be a drift of a small number of electrons forming a channel, which is shown here by high temperature values. The temperature varies within 500-600 K. When V_g of 1 V is supplied, more electrons move from source to drain, resulting in a lower temperature variation within 400-450 K. When the device is applied with V_g equal to 2 V, a large number of electrons will flow from source to drain, showing a temperature variation within 375-400 K. Since there is an inverse relationship between the temperature and the number of electrons (Fig. 8), it is evident that at

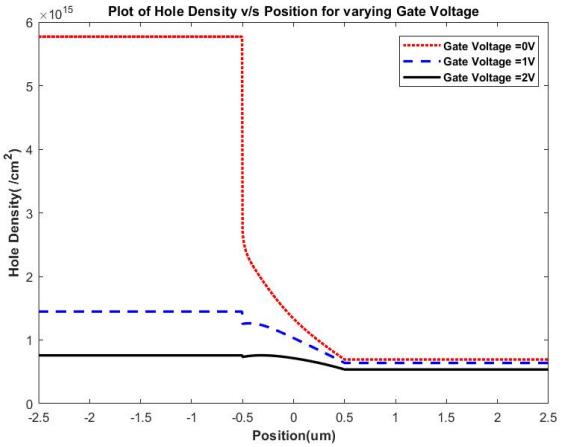

Fig. 6 – Variation of hole density in the channel region for different gate voltage

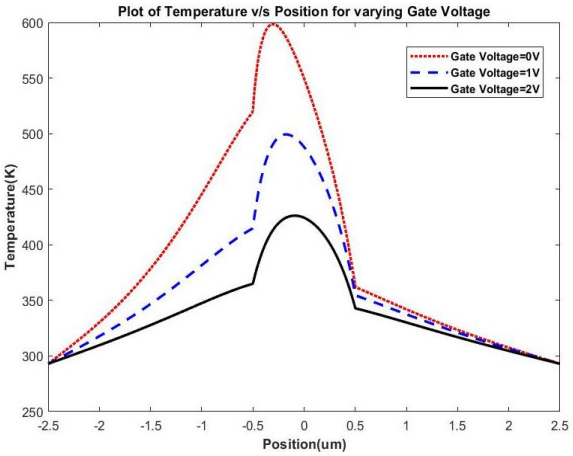

Fig. 7 – Variation of temperature in the channel region for different gate voltage

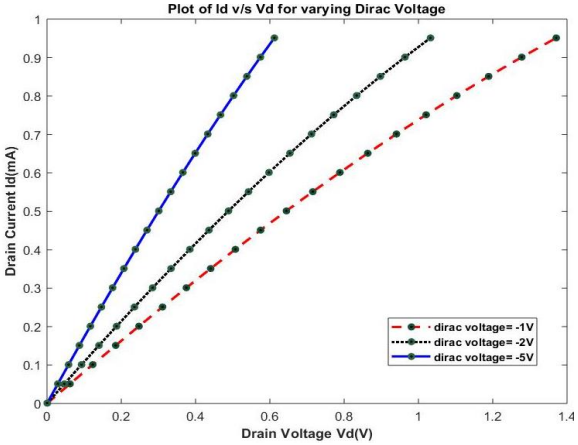

Fig. 8 – Variation of drain current for different Dirac voltages

large V_g values the electron flux will be greater, hence high temperatures will be unfavorable.

Fig. 8 shows the change in drain current (I_d) with drain voltage (V_d) for different Dirac voltage. The current in milliampere (mA) along the vertical axis varies with voltage in volt (V) along the horizontal axis. Dashed lines indicate a Dirac voltage of – 1 V, dotted lines indicate a Dirac voltage of – 2 V, and solid lines indicate a Dirac voltage of – 5 V. The curve for all three cases shows direct proportionality between the axes. For a Dirac voltage of – 1 V, the Dirac point of graphene shifts, leading to drain current. From Fig. 8, for a drain voltage of 1.4 V, the device reaches its peak value of 1 mA. Similarly, for a Dirac voltage of – 2 V, there is a shift in the Dirac point of graphene, the device reaches its peak value (1 mA) for a drain voltage of 1 V. As the Dirac voltage is further increased to a more negative value, – 5 V, there is a significant shift of the Dirac point, influencing more and more electrons to drift towards the conduction band, producing a large drain current i.e., the device reaches its peak value (1 mA) for a drain voltage of 0.5 V.

4. CONCLUSIONS

The study of the nanodevice structure shows an improvement in the sensitivity characteristics with drain current operation. The device is modeled for various simulations, which contributes to the overall gain of the device. The channel length reduction, which is the key for performance improvement, is achieved i.e., the device has an improved drain current for a channel length of 0.5 μm compared to 1 μm. Drift is required for the channel formation; the gate voltage is also reduced to improve drain current. Mobility phenomenon contributing to the drain current is shown. The gate voltage, which controls charge carriers leading to drain current, is observed. The proportionality between operating temperature and electron flow is proved, and the optimum temperature for better performance is 293 K. The Dirac point, which is a vital part of graphene characteristics, is shifted, and for a Dirac voltage of – 5 V, the drain current works best.

REFERENCES

1. Ethan Mallick, *IEEE Annal. History Comput.* **28** No 3, 62 (2006).
2. K. Roy, S. Mukhopadhyay, H. Mahmoodi-Meimand, *Proc. IEEE*, **91** No 2, 305 (2003).
3. P. Vimala, N.B. Balamurugan, *COMPEL: The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, **33** No 1/2, 630 (2014).
4. Erik P. Debenedictis, *Computer: the Flagship Publication of the IEEE Computer Society* **50** No 2, 72 (2017).
5. P. Vimala, Manjunath Bassapuri, Krishna Maheshwari, *2019 4th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT)*, 125 (Mysuru: IEEE: 2019).
6. P. Vimala, N.R. Nithin Kumar, *J. Nano Res.* **59**, 137 (2019).
7. P. Vimala, N.B. Balamurugan, *J. Electrical Eng. Technol.* **9** No 2, 649 (2014).
8. P. Vimala, Krishna Maheshwari, *J. Nanotechnol. Nano-Eng.* **5**No 2, 19 (2019).
9. P. Vimala, N.B. Balamurugan, *J. Semiconductors* **33**, No 3, 034001 (2012).
10. P. Vimala, S.S. Sharma, L. Likith Krishna, Manjunath Bassapuri, Thiruveedi Manikanta, *2020 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT),* 1 (Bangalore: IEEE: 2020).
11. Y.Q. Wu, Y.M. Lin, K.A. Jenkins, J.A. Ott, C. Dimitrakopoulos, D.B. Farmer, F. Xia, A. Grill, D.A. Antoniadis, P. Avouris, *2010 IEEE International Electron Devices Meeting (IEDM),* 9.2.1 (San Francisco: IEEE: 2010).
12. J.D. Aguirre-Morales, S. Frégonèse, C. Mukherjee, C. Maneux, T. Zimmer, *IEEE Trans. Electron Dev.* **62** No 12, 4333 (2015).
13. F. Schwierz, *Proc. IEEE* **101** No 7, 1567 (2013).
14. Sengupta Sujoy, Aravind Dev, Someeshwar, Richardson Vimal, B. Bala Tripura Sundari, *International Journal of Electronics and Communication Engineering* **7**, 81(2014).
15. S. Fregonese et al., *IEEE Trans. Nanotechnol.* **12** No 4, 539 (2013).

Вивчення нової структури пристрою: польовий транзистор на графені (GFET)

P. Vimala[1], Manjunath Bassapuri[1], C.R. Harshavardhan[1], P. Harshith[1], Rahul Jarali[1], T.S. Arun Samuel[2]

[1] *Department of Electronics & Communication Engineering, Dayananda Sagar College of Engineering, Shavige Malleshwara Hills, Bengaluru, 560078 Karnataka, India*
[2] *National Engineering College, Kovilpatti, 628503 Tamil Nadu, India*

Метою роботи є підвищення продуктивності нанопристроїв, що в цілому дає переваги електронним додаткам. Продуктивність при низькому споживанні енергії, висока чутливість і більша швидкість перемикання є необхідними умовами сучасної ери електроніки. Запропонована робота визначає тривимірну структуру польового транзистора на графені (GFET). Зазначена структура перебуває в еволюційній фазі і досліджується щодня. Основні переваги пристрою з точки зору загальної продуктивності і конкретних додатків зробили цікавим його детальне дослідження. Структура графену забезпечує виняткові можливості для його роботи і, отже, є відмінним рішенням для сенсорних додатків. Графен розміщується між витоком і стоком, утворюючи міст і забезпечуючи шлях для руху електронів. Нанопристрій моделюється для таких електричних параметрів, як струм стоку, напруга стоку, напруга Дірака, рухливість, густина електронів, густина дірок, температура. Пристрій моделюється за допомогою інструменту моделювання NanoHUB. Запропоновано поведінку струму стоку при зміні довжини каналу і напруги на затворі. Спостерігаються поліпшені характеристики пристрою при змен-

шенні довжини каналу, напруги на затворі та зсуву точки Дірака. Точка Дірака відіграє життєво важливу роль у механізмі провідності графену, а отже, і GFET. Для даних параметрів моделювання вивчали точку Дірака і спостерігали її зсув, що призводило до зміни провідності. Варіацію струму стоку було змодельовано для різних напруг стоку, що дало достатні докази ефективності і, отже, низького енергоспоживання. Розподіл носіїв та різних робочих температур уздовж каналу представлено для змінної напруги на затворі. Результати показують перевагу GFET для сьогоднішніх потреб в сенсорних додатках.

Ключові слова: NanoHUB, Графен, GFET, Рухливість, Струм стоку.