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An electronic architecture for intelligent portable pulse-echo ultrasonic instrument

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Abstract – experimental evaluation of several pulse-echo ultrasonic instruments developed in our laboratory to date for liquid foodstuffs testing and monitoring has identified a need for a new design. This design aims to reduce the required measurement time and size of the instrument by modifying its electronic architecture in terms of components used, configuration of programmable logic and firmware.

Ultrasound pulse-echo sensing is used, i.a., for detection of distant objects underwater (sonars), imaging of biological tissues and fluids (medical ultrasound) and non-destructive evaluation (NDE) of properties of natural and artificial structures and materials. In the latter two cases higher spatial resolution is achieved by using ultrasound waves at above 1 MHz. This frequency makes it difficult to use conventional microprocessors for data acquisition. Therefore field programmable gate arrays (FPGAs) are used instead.

Accuracy of the acquired waveforms to a large extent depends on the analog-to-digital converter (ADC) sampling frequency and the additive noise level. As the pulse-echo waveforms of interest can be excited at will, the waveform accuracy can be improved by using interleaved sampling and waveform averaging [1]. A typical structure of an ultrasonic pulse-echo instrument is presented in fig.1 (AFE stands for analogue front end that interfaces the FPGA and ADC to the ultrasound transducer).

Several FPGA-based instruments were developed in the applied ultrasonics laboratory of the Nottingham University to date (table 1, excluding the last line). The ultimate goal of these efforts was to develop a robust, affordable and portable intelligent instrument for a range of ultrasonic NDE applications. Original successful designs were implemented using the Xtreme DSP development kits [1]. The successive developments aimed at using a lower specification FPGA to reduce the instrument's cost. The first Spartan 3 design was largely accomplished as a proof of concept [2]. It uses two different boards (an FPGA board and an evaluation ADC board) connected by a custom

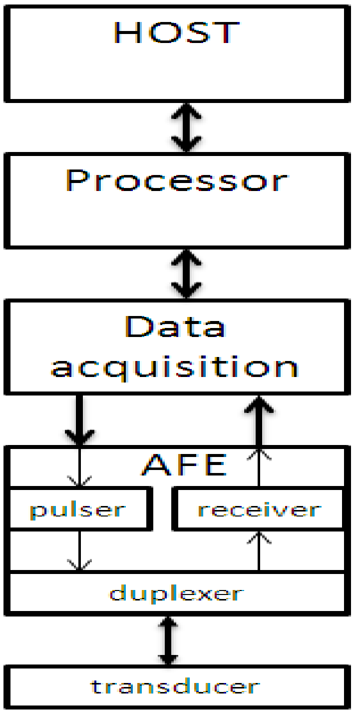

Fig.1. Structure of an ultrasonic NDE pulse-echo system

Table I. Comparison of designs

Interface	Host	Processor	Data acquisition	ADC freq, MHz	Memory, samples	Xilinx tools	AFE	Form factor	Cost	Ref
PCI+ DMA	PC		XC2V3000 Virtex II	80	24k / 32b	6.3	UPR[1]	PC board+ UPR[1]	High	[1]
PCI+ DMA	PC		XC2VP30 Virtex II Pro	100	36k / 32b	7.1	UPR[1]	PC board+ UPR[1]	High	
JTAG	PC		XC3S400 Spartan3	40	1k / 32b	6.3	Custom	FPGA board + ADC board	£400	[2]
RS-232	PC	XC3S500 Spartan3		50	20k / 16b	8.2	Custom	FPGA board + custom AFE/ADC	£300	[3]
USB	*PC*	*XC3S500 Spartan3*		*100*	*100k / 16b*	*8.2*	*Custom*	*FPGA module +custom AFE/ADC*	*£250*	

[1] Ultrasonic pulser-receiver, NDT Solutions Ltd (UK)

PCB. Very limited capacity of the memory available for this Spartan part ruled out sophisticated applications suitable to the Virtex boards. Additionally, both additive noise and frame jitter levels were found over an order of magnitude higher than these for the Virtex boards. The most recent completed development utilized flexible interleaved sampling and embedded processing of the acquired waveforms that allowed changing data acquisition parameters without reconfiguring the FPGA and achieved up to 5 complete processed delay readings per second [3].

Although the progressively improved instruments were successfully applied to monitoring of some chemical and biological processes (e.g., [2, 3]), their recent application to the safety control and monitoring of liquid foodstuffs [4] identified a room for the following improvements: shorter measurement time and smaller size of the instrument.

In the design that is being undertaken at the moment these improvements will be addressed as follows:

- measurement time: reduction of required number of averages by using lower noise receiver and additional digital filtering of the acquired waveforms; reduction of the required interleaving factor by doubling the ADC sampling frequency; reduction of the processing time by modifying the firmware;
- physical size: use of an FPGA module instead of previously used FPGA development boards.

We anticipate that the present development will result in an intelligent portable pulse-echo ultrasonic instrument with the parameters presented in table 1, last line.

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